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CHAPTER 1  SPECIFICATIONS

(FB-500 Series)
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## 1-1 Major Specifications

<table>
<thead>
<tr>
<th>Model Name</th>
<th>FB-501</th>
<th>FB-502</th>
<th>FB-503</th>
<th>FB-504</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Single-side</td>
<td>Single-side</td>
<td>Double-side</td>
<td>Double-side</td>
</tr>
<tr>
<td>Items</td>
<td>Unit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory Capacity (MFM)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unformatted Per Disk</td>
<td>Bytes</td>
<td>250K</td>
<td>500K</td>
<td>1M</td>
</tr>
<tr>
<td>Formatted Per Disk</td>
<td>Bytes</td>
<td>164K</td>
<td>328K</td>
<td>656K</td>
</tr>
<tr>
<td>Basic Bytes/Sectors</td>
<td></td>
<td>256</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Format Sectors/Track</td>
<td></td>
<td>16 (Soft Sector)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Track OD mm</td>
<td></td>
<td>57.151</td>
<td></td>
<td></td>
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<td>Radius ID mm</td>
<td></td>
<td>36.514</td>
<td>36.249</td>
<td>34.396</td>
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<tr>
<td>Media Number of Recording Sides</td>
<td>1</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cylinders</td>
<td>40</td>
<td>80</td>
<td>40</td>
<td>80</td>
</tr>
<tr>
<td>Number of Tracks</td>
<td>40</td>
<td>80</td>
<td>160</td>
<td></td>
</tr>
<tr>
<td>Index</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Recording Method</td>
<td>FM/MFM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Packing Density BPI</td>
<td>5536</td>
<td>5576</td>
<td>5876</td>
<td>5922</td>
</tr>
<tr>
<td>Track Density TPI</td>
<td>48</td>
<td>96</td>
<td>48</td>
<td>96</td>
</tr>
<tr>
<td>Data Transfer Speed Bits/sec</td>
<td></td>
<td>125K/250K</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Access Time Average Latency msec</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Seek Time msec</td>
<td>6</td>
<td>3</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>Settling Time</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>Average Access Time msec</td>
<td></td>
<td>88</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Head Load Time msec</td>
<td></td>
<td>Option (35ms)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Motor Starting Time msec</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spindle Speed RPM</td>
<td></td>
<td>300</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This drive has been designed conforming to the media specified in ISO, ANSI, ECMA, and JIS.
1-2 Mechanical Dimensions and Installation

(1) Width  	146mm (5.75 Inches)
(2) Height  	41mm (1.61 Inches)
(3) Depth  	204mm (8.03 Inches)
(4) Dimensions  
(5) Weight  	1.4Kg
(6) Cooling System  
Natural Air Cooling
(7) Installation  
3 Ways (See Fig. 1-1)

1. Vertical Mount: LED lamp up or down.  [Fig (a) or (b)]
2. Horizontal Mount: Drive Motor down.  [Fig (c)]

Fig. 1-1 Installation.

NOTE: Use the mounting holes in the side frames or bottom frame of the FDD with M3 screws. (See Fig. 1-2)
M3 screw hole locations on the side frames.

M3 screw hole locations on the bottom frame.

NOTE: All dimensions are in mm.
Dimensions in ( ) are in inches.
1-3 Physical Specifications

(1) Ambient Temp.
   (a) Operating 5 to 45°C (10 to 52°C for media. Refer to the ISO Specifications).
   (b) Shipping -40 to 60°C
   (c) Storage -22 to 53°C

(2) Relative Humidity
   (a) Operating 20 to 80%RH (Non-condensing)
   (b) Non-operating 8 to 90%RH (Non-condensing)
   (c) Max Wet-bulb Temp. 29°C (84°F)

(3) Vibration
   (a) Operating Acceleration : Less than 0.25G (10~25Hz)
   (b) Shipping Acceleration : Less than 2G (Less than 100Hz)

(The unit must be packaged as per the TEC standard.)

(4) Shock
   (a) Shipping Acceleration : Less than 40G (Less than 10ms)

(The unit must be packaged as per the TEC standard.)

(5) Dust
    The drive should not be used in a dusty location.
### 1-4 Power Requirements

(1) +12V DC

(a) Tolerance : ±5%
(b) Ripple Voltage : Less than 100mV P-P
(c) Average Load Current : Approx. 0.7A (with head load mechanism)
                           0.5A (without head load mechanism)
(d) Surge Current : 1A (200msec at spindle motor start-up)

(2) +5V DC

(a) Tolerance : ±5%
(b) Ripple Voltage : Less than 50mV P-P
(c) Average Load Current : Approx. 0.5A
(d) Max. Load Current : Less than 0.7A

### 1-5 Reliability

(1) Mean Time Between Failures (MTBF) : 10000 Power On Hours

(2) Mean Time to Repair (MTTR) : 30 minutes

(3) Error Rates

  (a) Soft Read Errors : Less than one error per $10^9$ bits read.
  (b) Hard Read Errors : Less than one error per $10^{12}$ bits read.
  (c) Seek Errors : Less than one error per $10^6$ seeks

(4) Media Life : More than $3 \times 10^6$ passes/track

(5) Media Insertions : More than $3 \times 10^4$ times
CHAPTER 2 CONSTRUCTIONS

The unit consists of the following components.

2-1 Magnetic Head

The single-side magnetic head uses a button type head and the double-side magnetic head uses a gimbal type, both using the tunnel erase method.

2-2 Head Positioning Mechanism

The head is positioned by the rotation of the stepping motor through the steel belt.

2-3 Head Load Mechanism for double-sided type only (Option)

The mechanical method by a small solenoid and return spring.

2-4 Disk Drive Mechanism

The diskette rotation mechanism uses the DC brushless direct-drive motor to directly rotate the spindle at 300rpm.

2-5 Read/Write and Control Electronics

The read/write and control electronics include the following circuits.

(1) Index/sector detection circuit
(2) Drive circuit for head-load solenoid
(3) Drive circuit for head positioning stepping motor
(4) Track 00 detection circuit
(5) Write enable notch detection circuit
(6) Read-write circuit
(7) Drive select circuit
(8) Side select circuit
(9) Spindle motor control circuit

The diagram for read/write and control electronics is shown in Fig. 2-2.
Fig. 2-1 Block Diagram
Fig. 2-2 Electrical Block Diagram
CHAPTER 3 INTERFACE

The layout drawing of the interface is shown in Fig. 3-5. The interface is divided into a signal interface, power interface and frame ground.

3-1 Signal Interface

The signal line is negative logic TTL compatible.

(1) Input circuit  
See Fig. 3-1

(2) Output circuit  
See Fig. 3-2

(1) Input

\[ \text{FDD} \quad +5V \quad 150\Omega \quad \text{FDD} \]

TI SN74LS14/7414 or equivalent

\[ \text{HOST} \]

TI SN7438 or equivalent

Fig. 3-1 Input

(2) Output

\[ \text{FDD} \quad +5V \quad 150\Omega \quad \text{FDD} \]

TI SN7438 or equivalent

\[ \text{HOST} \]

TI SN74LS14/7414 or equivalent

Fig. 3-2 Output
(3) Signal Level

(a) Input Signal Level

Low Level (True) : 0V~0.4V (Flow out current of less than 40mA)
High Level (False) : 2.5V~5.25V

(b) Output Signal Level

Low Level (True) : 0V~0.4V (Sink current of less than 48mA)
High Level (False) : 2.5V~5.25V

(4) I/O Signal and Pin Location

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Signal</th>
<th>Signal Name</th>
<th>Signal Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>1</td>
<td>2</td>
<td>NC</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>*[IN USE OR HEAD LOAD]</td>
<td>←</td>
</tr>
<tr>
<td>5</td>
<td>6</td>
<td>DRIVE SELECT 3</td>
<td>←</td>
</tr>
<tr>
<td>7</td>
<td>8</td>
<td>INDEX/SECTOR</td>
<td>←   →</td>
</tr>
<tr>
<td>9</td>
<td>10</td>
<td>DRIVE SELECT 0</td>
<td>←</td>
</tr>
<tr>
<td>11</td>
<td>12</td>
<td>DRIVE SELECT 1</td>
<td>←</td>
</tr>
<tr>
<td>13</td>
<td>14</td>
<td>DRIVE SELECT 2</td>
<td>←</td>
</tr>
<tr>
<td>15</td>
<td>16</td>
<td>MOTOR ON</td>
<td>←</td>
</tr>
<tr>
<td>17</td>
<td>18</td>
<td>DIRECTION</td>
<td>←</td>
</tr>
<tr>
<td>19</td>
<td>20</td>
<td>STEP</td>
<td>←</td>
</tr>
<tr>
<td>21</td>
<td>22</td>
<td>WRITE DATA</td>
<td>←</td>
</tr>
<tr>
<td>23</td>
<td>24</td>
<td>WRITE GATE</td>
<td>←</td>
</tr>
<tr>
<td>25</td>
<td>26</td>
<td>TRACK 00</td>
<td>←   →</td>
</tr>
<tr>
<td>27</td>
<td>28</td>
<td>WRITE PROTECT</td>
<td>←   →</td>
</tr>
<tr>
<td>29</td>
<td>30</td>
<td>READ DATA</td>
<td>←   →</td>
</tr>
<tr>
<td>31</td>
<td>32</td>
<td>SIDE SELECT</td>
<td>←</td>
</tr>
<tr>
<td>33</td>
<td>34</td>
<td>*[READY]</td>
<td>←   →</td>
</tr>
</tbody>
</table>

Table 3-3 I/O Pin Location Table * Option
(5) Signal Connector

(a) Number of Pins  34

(b) Edge Card Connector on FDD

![Diagram of Edge Card Connector]

Fig. 3-4 Drawing of Edge Card Connector  NOTE: All dimensions are in mm. Dimensions in ( ) are in inches.

(c) Mating Connector: See Fig. 3-5.
A14D.

P/N' 60972-7 or equivalent

PC Board

I/O Cable Receptacle

Mating Plug

AMP. P/N 583717-5 (Housing)
P/N 1-583616-1 (Pin)
P/N 583274-1 (Keying plug)
P/N 3463-0001 (Connector)
P/N 3439-0000 (Keying plug)

Twisted Cable : AMP

Flat Cable : 3M

Fig. 3-5 Interface Layout
3-1-1 Input Signal Lines (FDD ← HOST)

(1) DRIVE SELECT 0 - 3

When one of four lines becomes LOW, only the drive with LOW signal will respond to the input lines, gate the output lines and turn the LED on.
Up to four drives can be controllable, and DRIVE SELECT (0~3) is pre-determined by shorting plug. (See Fig. 5 - 3).

(2) DIRECTION

This line is a control signal which defines direction of R/W head motion. If the input signal is LOW, the R/W head will move towards the center of the disk (STEP IN).
Conversely, if the input signal is HIGH, the R/W head will move away from the center of the disk (STEP OUT).
Any change in the DIRECTION must be made before receiving STEP pulse. (See Timing Chart)

(3) STEP

This signal is to move the R/W head by one track per one pulse. After receiving the final STEP pulse, the drive must wait at least Seek + Settling time to enable Read/Write securely.

(4) SIDE SELECT

This signal defines which side of a two-sided diskette to be written on or read from.
When this signal is LOW, side 1 head is selected, and when HIGH, side 0 head is selected. When switching from one side to the other, the waiting time is required before read/write operation starts.
At the write operation, this signal must remain the same until the tunnel erasure is completed. (See Timing Chart)
(5) WRITE GATE

LOW level enables write data to be written on the diskette. This signal becomes ineffective when WRITE PROTECT signal is LOW or the drive is not selected. HIGH level enables to read the data on the diskette.

(6) WRITE DATA

This line provides data to be written on the diskette. Each transition from HIGH to LOW of the FM/MFM signal will reverse the current through the R/W head, thereby writing a data bit. This line is enabled when WRITE GATE is LOW, WRITE PROTECT is HIGH and DRIVE SELECT is LOW.

(7) MOTOR ON

When this signal is LOW, the spindle motor rotates and when HIGH, the motor stops. The spindle motor reaches to the rated speed within 0.5 second. This line responds to the input signal regardless of the DRIVE SELECT signal.

(8) HEAD LOAD (Option for double-sided version only)

This signal line is used either HEAD LOAD or IN USE. When this signal is low, R/W head loads against the diskette. The set-up time of the solenoid is required before using this signal. This signal line responds to the input signal regardless of DRIVE SELECT line.

(9) IN USE (Option)

When DRIVE SELECT signal is low, LOW level of this line will turn the LED on and HIGH will turn the LED off.
Output Signal Lines (FDD → HOST)

1. INDEX/SECTOR
   The LOW signal is provided by the drive once each revolution of the diskette to indicate the beginning of the track.

2. READ DATA
   This line provides clock + data pulses which are converted from analog data detected by a R/W head.

3. TRACK 00
   The LOW state of this signal indicates that the R/W head is positioned at track 00.

4. WRITE PROTECT
   The LOW signal indicates that a write protected diskette is installed.
   The drive will inhibit writing with a write protected diskette.

5. READY (Option)
   The LOW signal indicates that the diskette is rotating after properly inserted.
3.2 Power Interface

Power Connector

(a) Number of Pins : 4

(b) Power Connector Pins : See Fig. 3-6

(c) Mating Plug (Host Side) : AMP P/N 1-480424-0

(d) Mating Pin (Host Side) : AMP P/N 170148-2 (AWG18 ~ 24)
AMP P/N 170121-4 (AWG14 ~ 20)

3.3 Frame Ground

Mating Terminal (Host Side) : AMP P/N 60972-1

NOTE: Use AWG24 or thicker cable for the power cable and ground cable.

PC board

1 PIN ------- DC +12V
2 PIN ------- OV RETURN (GROUND)
3 PIN ------- OV RETURN (GROUND)
4 PIN ------- DC +5V

Fig. 3-6 Power Connector Pins
Fig. 3-7 Interface Connections
Chapter 4 Timing Chart

Fig. 4-1 Track Access Timing
FB-501,503 6 ms min.
502,504 3 ms min.

Fig. 4-2 Read Data Timing
FB-501,503 21 ms min.
502,504 18 ms min.
Fig. 4-3 READ DATA

READ DATA (FM)

C D C D C D C D C D

8µs nom.

4µs nom. ± 250ns

READ DATA (FM)

C C D D D D D

4µs nom.

6µs nom.

1µs ± 250ns

8µs nom.

Fig. 4-3 READ DATA

DRIVE SELECT

STEP

HEAD LOAD

WRITE GATE

SIDE 1 SELECT

WRITE DATA

1ms min.

35ms min.

1ms min.

35µs min.

lms min.

lms min.

lms min.

8µs max.

8µs max.

*** = Seek Settling Time

FB-501, 503 21 (ms) min.

502, 504 18 (ms) min.

Fig. 4-4 Write Data Timing
WRITE DATA (FM)

250ns min. 4us±20ns 8us±40ns
2100ns max.

WRITE DATA (MFM)

250ns min. 6us±30ns 8us±40ns
2100ns max. 4us±20ns

Fig. 4-5 WRITE DATA TIMING

INDEX

3ms nom.

200ms

Fig. 4-6 INDEX TIMING
CHAPTER 5 SELECT PIN SETTING

5-1 Input Signal Termination

FB-500 can be connected either daisy chain or radial chain. Each drive has the line termination network (terminator). As shipped from the factory, the terminator is installed on each drive. Remove this network when not necessary. Daisy chain and radial chain are shown in Fig. 5-1 and 5-2 while the location of terminator is shown in Fig. 5-3.

5-2 FDD Number Shorting plug

The address of each drive is determined by the location of shorting plug. As shipped from the factory, a shorting plug is installed on the DRIVE SELECT 0. (See Fig. 5-3)

5-3 Shorting Plug for Testing (MX)

The output signal is always effective regardless of the DRIVE SELECT 0 ～ 3 signals. (See Fig. 5-3)
Fig. 5-1 Daisy Chain

Only the FDD 3 must have the line terminator.

Fig. 5-2 Radial Chain Method

Each FDD must have the line terminator.

Fig. 5-3 FDD No. Setting and Terminator

Terminator (DIP14pin)

FDD No. Shorting Plug and MX Terminal
Chapter 2 Mechanical Section

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1. DISK PROTECTION MECHANISM AND CLAMP MECHANISM

(1) The FB-503 and FB-504 are so designed that the door cannot be locked until the disk is completed inserted in the unit. In the FB-501 and FB-502, the head cannot touch and damage the disk because it is a single-side head.

(2) The clamp mechanism of the FB-500 Series accurately centers the disk to protect the center hole of the disk, thus lengthening the life of the disk.

(3) The shape of the front panel allows the disk to be inserted or removed easily.
2. INSTALLATION AND REMOVAL OF COMPONENTS

2.1 PC Board

(1) Removal of PC Board
- Remove the three set screws retaining the PC board to the base.
- Detach all the connector cables.

(2) Installation of the PC board
- Attach the connector cables to the PC board. Make sure that the connector cables are properly routed. In the case of the double-side head, be extremely careful to distinguish the upper from lower head cables. The cables of the upper head should be white-marked.
- Tighten the three set screws of the PC board.
- The write protector and index sensor are directly mounted on the PC board. The write protector requires almost no adjustment while it is necessary to adjust the index sensor whenever it is mounted on the PC board. The index sensor should be adjusted by referring to page 2-8.
2.2 Clamp Base BK and Clamp Arm K

(1) Remove the PC board by referring to the section 2.1 (page 2-2).

(2) Remove the set screw retaining the clamp lever, and pull out the clamp lever from the shaft. Pull out the pin inserted in the shaft.

(3) Remove the four set screws retaining the clamp base BK.

(4) Pull out the clamp lever shaft by removing the E-ring and clamp lever spring.

(5) In the above procedure, the clamp arm K parts from the clamp base BK.

(6) The clamp BK can be removed by separating the clamp base BK from the base and pushing down the clamp arm.

(7) Follow the above procedure in reverse for re-assembly.
2.3 Carrier BK

(1) Remove the PC board by referring to the section 2.1 (page 2-2).

(2) Remove the clamp base BK by referring to the section 2.2 (page 2-3).

(3) Remove the two screws connecting the belt supporter to the carrier BK.

(4) Remove the head cable.

(5) Remove the set screws of the shaft holders OUT and IN, and remove the shaft holders OUT and IN.

(6) Remove both carrier shafts.

(7) When re-mounting the carrier, the adjustment requirements must be performed.

(8) Follow the above procedure in reverse for re-assembly.
(1) Remove the carrier BK from the base by referring to section 2.3 (page 2-4).

(2) Remove the screws positioning and retaining the pulse motor K.

(3) Remove the set screws of the belt supporter.

(4) Remove the pulley set screw of the pulley, which is retaining the belt.

(5) Follow the above procedure in reverse for re-assembly, after adjusting the steel belt tension.
2.5 Spindle Motor K

(1) Remove the PC board by referring to the section 2.1(page 2.2)

(2) Remove the clamp base K and clamp arm K by referring to section 2.2(page 2.3).

(3) Remove the three set screws holding the spindle.

(4) Follow the above procedure in reverse for re-assembly.
2.6 Interrupter and Adjustment of Track00

(1) Remove the FC board by referring to the section on 2.1(page 2.2)

(2) Remove the positioning set screw of the interrupter AK.

(3) Remove the interrupter.

(4) Temporarily tighten the positioning set screw when mounting the interrupter.

(5) Perform the TROO adjustment in section 3.
3. ADJUSTMENT

3.1 Index Sensor Adjustment

(1) The index sensor optically detects the index hole in the disk.

(2) The index sensor should be adjusted in the following manner.

a. The LED of the index sensor is built in the DD motor K thus it cannot be adjusted in position.

b. The photo transistor is adjusted by loosening the socket screw.

c. Use a commercially available alignment diskette. The alignment diskette usually stores the index burst signal at two points, the outer track and inner track.

d. Connect the CH1 probe of the oscilloscope to pin 2 of TP-1, and the CH2 probe to pin 3 or 4 of TP-2. Connect the GND to pin 4 of TP1 or pin 2 of TP-2. (CH level: 40mV/div.d.c., time base: 50μs/div.)

e. The index burst signal appears as follows:

   Outer Track: Within 200μs ± 100μs
   Inner Track: Within above 50μs

f. Move and adjust the transistor in position to meet the above values.

   o For a double-side machine, make adjustments until both sides meet the above values.
3.2 Tensioning and Adjustment of Steel Belt

(1) Remove the pulse motor BK by referring to the section 2.4 (page 2.5).

(2) Loosen the socket bolt for positioning the pulse motor and pulley, and pull out the pulley from the shaft of the pulse motor.

(3) Use the independent tool to tension and adjust the steel belt.

(4) Set the pulley on the jig, wind the belt round the pulley, and temporarily fix the pulley and belt with the set screw.

(5) Set the belt as shown in the figure, temporarily fix the right end belt holding screw. Pull the left end of the belt by a force of 1.2Kg with the tension gage, and then fasten the belt.

(6) When following step(5), be sure that the belt is wound in parallel with the pulley.

(7) Finally tighten the screw temporarily retaining the pulley and belt.

(8) Temporarily tighten the pulley and belt to the shaft of the pulse motor to provide excitation later.
3.3 Head/Radial Adjustment (CE Adjustment)

(1) Measure and adjust the reproduced signal waveform of track 16 (double track 32 for) of a commercially available alignment disk. At this time, observe the waveform by moving the carrier from outer side and inner side.

(2) Obtain the waveform shown in the figure above

(3) Externally trigger the fall of the index signal of pin 2 of TP-1. The waveform should be stationary.

(4) Connect CH1 to pin 2 of TP-2, and CH2 to pin 4 of TP-2, and GND to pin 4 of TP-1 or pin 2 of TP-2. (CH level: 50mV/div. d.c., time base: 20mS/div.)

(5) A temperature and humidity correction table is provided for the alignment disk in each maker. Adjust the measured value according to the table.

Measurement Reference

$$100\% \times \left(\frac{V_1}{V_2} \text{ or } \frac{V_2}{V_1}\right) \times 100\% = 85\%$$

Adjust to obtain the result of either of the above expressions.

Adjustment Points

For side 0 (lower head), make adjustments by moving the pulse to the right or left. For double sides, adjust the lower head first, then adjust side 1 (upper head) after switching the head. For the upper head, make adjustments by loosening the socket screws on the carrier and by moving the head to the right or left.
3.4 Head Output Adjustment

Follow the procedure below to adjust the head output.

(1) Use a disk which is normal and clean enough to detect any fault in the head.

(2) Start the motor.

(3) Write 2F signals on track 00 and track 39/79, and then reproduce them. Read the reproduced signal waveforms with the synchroscope.

(4) Obtain the waveform shown in the figure above. Use a synchroscope with two channels and an external trigger function.

(5) Connect the external trigger to pin 2 of TP-2 (5V/div., d.c.), and synchronize on the fall of the signal. Connect other channels 1 and 2 to pin 3 of TP-2 and pin 4 of TP-2 ground each probe. Set to ADD mode, set either pin 3 or 4 of TP-2 to INVERT, and set the time base at 20ms/div. Measure the average value of an area of at least 4 milliseconds as shown in the figure above.

(6) The adjustment criteria is for more than 900mV (single track) or 600mV (double track) amplitude with the 2F signal on track 39/79. Adjust by loosening the set screw of the pulse motor and changing the position of the pulse motor.

(7) Modulation: 

\[ M = \frac{V_{\text{max}} - V_{\text{min}}}{V_{\text{max}} + V_{\text{min}}} \times 100\% \]

2-11
3.5 Motor Speed Adjustment

(1) Insert the media after the motor ON signal is inputted.

(2) Adjust VR1 on the DD motor control PC board so that the black stripe of the stroboscope of the DD motor looks stationary under a 50Hz- or 60Hz-fluorescent lamp. The DD motor used is shown below.
3.6 Track 00 Adjustment

* Adjustment of Track 00

- Make this adjustment after the CE is adjusted.

- Points to Which Probes Are Connected
  Connect CH-2 to pin 3 of TP-1, and CH-1 to pin 5 of TP-1. Pin 4 of TP-1 is connected to GND. The rise of the STEP signal emitted from pin 3 of TP-1 is synchronized.

- Adjustment Points
  Set the carrier so that it will run between Track 4 and Track 1. Make adjustments by moving the interrupter until the following timing is obtained.

<table>
<thead>
<tr>
<th>Track</th>
<th>STEP</th>
<th>ON</th>
<th>(max.)</th>
<th>OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>2.8m sec</td>
<td>2.8m sec</td>
<td>2-13</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3.7 Adjustment of Head Azimuth

1. This adjustment is possible only for side 1 (upper head).

2. Points to Which Probes Are Connected
   Connect the probe of CH-1 to pin 2 (INDEX) of TP-1 for synchronization. Connect the probe of CH-2 to pin 3 or pin 4 of TP-2.

3. Move the carrier to track 34 (68 in the case of double track) on the alignment disk, and make adjustments so that the following waveform will be obtained.

   ![Waveform Diagram]

   - C/B ≥ 73.5%
   - B/C ≥ 73.5%
   - B ≥ C
   - A ≥ B and D ≥ C

   More than 73.5% will be accepted.

   - Since the index burst, azimuth, and CE for side 1 must be adjusted by moving the head, move the head to a position where these three conditions are met.
4. SPECIAL MAINTENANCE TOOLS

The following special tools are used for maintenance.

<table>
<thead>
<tr>
<th>Tool Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>a. Oscilloscope</td>
<td>30MHz</td>
</tr>
<tr>
<td>b. Simulator</td>
<td>(Example: BRIKON)</td>
</tr>
<tr>
<td>c. DC supply</td>
<td>+12V, +5V</td>
</tr>
<tr>
<td>d. Alignment Diskette</td>
<td></td>
</tr>
</tbody>
</table>
5. MAINTENANCE

5.1 PROCEDURE FOR CLEANING THE READ/WRITE HEAD

In the FB-501, 502, 503 and 504, only the floppy disk head cannot be replaced, because it is completely bonded to the carrier. The head should be cleaned only when accumulated oxide compounds (r-Fe₂O₃) are noticeable. Note that any other cleaning method than the one described below may cause scratches on the head.

1. Slightly damp a cotton swab with isopropyl alcohol.
2. Part the load arm from the head without touching the load button.
3. Softly wipe the head with the dampened part of the cotton swab.
4. After the alcohol has fully evaporated, softly polish the head with a clean cotton swab.
5. Place the load arm on the head. At this time, extreme caution should be exercised to avoid shocks to the head.

5.2 Caution on Handling Disks

- Avoid directly touching the mylar.
- Avoid storing disks in locations with high temperature or high humidity.
- A disk should be taken out from or inserted into the drive while the power is on (while the DD motor is operating).
- Always ensure that the disk is inserted properly.
CHAPTER 3  CIRCUIT EXPLANATION

(FB-500 SERIES)
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3. ELECTRICAL DIAGRAM ....................................... 3
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   6.5 Read Amplifier Circuit ................................ 22
1. GENERAL DESCRIPTION

This circuit uses two independent LSIs: the LSI that controls the signals from the pulse motor, DD motor, and the sensors and the LSI for the read circuit, thus realizing an increase in packaging density, compaction of the unit, power-saving and improvement of the reliability.
2. BLOCK DIAGRAM

![Block Diagram Image]

- Drive Select 0
- Drive Select 1
- Drive Select 2
- Drive Select 3
- Track 00
- Index/Sector
- Motor ON
- Write Data
- Write Gate
- Write Protect
- Read Data
- Step
- Direction
- Side Select
  - In Use or
  - Head Load
  * Ready
  * Option

- Spindle Motor Control
- R/W Data (Side 1)
- R/W Data (Side 0)
- Head Position
- Track 00
- Head Load
- Index
- Motor ON
- Active Lamp
- Write Protect
- Index/Sector
3. ELECTRICAL DIAGRAM

MOTOR ON

Motor Control

Spindle Motor

Drive Select 0

Drive Select 1

Drive Select 2

Drive Select 3

Index/Sector

Index/Sector Logic

Index/Sector Sensor

* Ready

In Use or Head

Load

Step

Direction

Head LOAD Driver

Head Load Solenoid

Position Control Logic

Stepper Motor

Track 00

Track 00 Logic

Track 00 Sensor

Write Protect

Write Protect Logic

Write Protect Sensor

Write Gate

R/W Erase Control Logic

R/W Head 0

Erase Head 0

Write Data

Write Amplifier

Erase Head 1

R/W Head 1

Read Data

Read Amplifier

* Option

Side Select

* Option
4. INDEPENDENT LSI CONFIGURATION AND PIN NAMES

4.1 Control LSI

Provided with the same functions as a one-chip CPU, this independent LSI is designed considering the hard timing required by the flexible disk drive (hereinafter referred to as "FDD"). The package is made compact and operated from a single +5V supply. All the pins are TTL-compatible. This LSI mainly controls the logic system.

Pin Configuration
## Pin Names

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>R5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>R6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>R7</td>
<td>External Motor Rotation Signal</td>
</tr>
<tr>
<td>7</td>
<td>R8</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>R9</td>
<td>Write Gate Signal</td>
</tr>
<tr>
<td>9</td>
<td>R10</td>
<td>Write Gate Edge</td>
</tr>
<tr>
<td>10</td>
<td>K0</td>
<td>Write Protect Signal</td>
</tr>
<tr>
<td>12</td>
<td>K1</td>
<td>Drive Select Signal</td>
</tr>
<tr>
<td>14</td>
<td>K2</td>
<td>Direction Signal</td>
</tr>
<tr>
<td>16</td>
<td>K3</td>
<td>Side One Select Signal</td>
</tr>
<tr>
<td>26</td>
<td>00</td>
<td>Pulse Motor Phase A</td>
</tr>
<tr>
<td>28</td>
<td>01</td>
<td>Pulse Motor Phase B</td>
</tr>
<tr>
<td>29</td>
<td>02</td>
<td>Pulse Motor Phase C</td>
</tr>
<tr>
<td>31</td>
<td>03</td>
<td>Pulse Motor Phase D</td>
</tr>
<tr>
<td>32</td>
<td>04</td>
<td>Track 00 External Output Signal</td>
</tr>
<tr>
<td>33</td>
<td>05</td>
<td>Ready Signal</td>
</tr>
<tr>
<td>34</td>
<td>06</td>
<td>Erase Gate Signal</td>
</tr>
<tr>
<td>36</td>
<td>07</td>
<td>Write Gate Signal Start and End Judgement</td>
</tr>
<tr>
<td>38</td>
<td>R0</td>
<td>For Pulse Motor Voltage Switching</td>
</tr>
<tr>
<td>40</td>
<td>R1</td>
<td>Track 00 Position</td>
</tr>
<tr>
<td>44</td>
<td>R2</td>
<td>Index Pulse</td>
</tr>
<tr>
<td>46</td>
<td>R3</td>
<td>Step Pulse</td>
</tr>
<tr>
<td>48</td>
<td>R4</td>
<td></td>
</tr>
</tbody>
</table>
4.2 Read LSI Configuration and Pin Names

This LSI is a monolithic read amplifier that outputs signals recorded on the floppy disk in the form of digital signals. The LSI amplifies signals from the magnetic head and passes them through the filter. Then, it passes them through the differentiator, zero volt comparator and waveform shaper to obtain pulse outputs.

Features

Floppy Disk read processing is performed by one IC. The outputs can be directly connected a TTL device.

**Pin Configuration**

| Amp Inputs Offset Decoupling Gnd One Shot Components One Shot Components |
|----------------|-----------------|----------------|-----------------|-----------------|-----------------|-----------------|
| 1              | 2               | 3              | 4               | 5               | 6               | 7               |
| 8              | 9               | 10             | 11              | 12              | 13              | 14              |
| 15             | 16              | 17             | 18              | 19              | 20              | 21              |

Vcc 2

**Block Diagram**

- 12V
- Amplification
- Analog Input Gain Select
- Amplifier
- Differentiator
- Comparator
- Peak Detection
- Shaping D.F.F
- Pulse Generator
- One-Shot
- Digital Output
- One-Shot 1, One-Shot 2
- 5V
5. INPUT SIGNAL LINES (CPU to FDD)

5.1 Drive Select Circuit

When one of these four signal lines goes low, the FDD corresponding to the low level line responds to other input signals, and further the gate of the output signal line of the FDD opens.

Up to four FDDs are controllable. Which of DRIVE SELECT 0~3 the FDD corresponds to is selected by inserting one short plug in the FDD. When selected by the shorting jumper, the "Low" level DRIVE SELECT signal is input to pin 12 of IC8 to place the CPU (control LSI) in a selected state. Also, this signal allows the LED on the front panel to illuminating through the motor driver (IC6).
5.2 Side Select Circuit

This circuit is used to select either side 0 or side 1 head. A low on this input signal line causes side 1 head to be selected and a high on this line causes side 0 head to be selected. Waiting time is required between the instance at which the selection is completed upon the change of the SIDE SELECT signal and the instance at which write/read is enabled. However, this signal must not be changed until the erasing is completed after the completion of writing because of the tunnel erase system employed. For the tunnel erase system, refer to (2) in section 5.6 Erase Circuit.
5.3 Head Positioning Circuit

The head positioning circuit is configured as shown above.

This circuit is used to move the head using step pulses, after the head stepping direction (inner or outer direction) is determined by the Direction signal. When the Direction signal from the host computer goes low and a step pulse signal is inputted, the head steps one track in the inner direction. When the Direction signal goes high, the head steps in the outer direction.

The timing chart for the Direction signal and Step signal is shown below.

In writing or reading data, it is necessary to wait for seek + setting time after the final step signal to stabilize the head.
5.4 WRITE GATE Signal

When the WRITE GATE input signal line of this circuit is low, the write circuit is made operable. However, writing will not occur, when the WRITE PROTECT output signal line is low (in a write disable state) or the corresponding FDD is not selected by the DRIVE SELECT signal line. When this input signal line is high, the FDD is in the read mode.

5.5 WRITE DATA Signal

This input signal line is used to transfer data to be written on the disk.

When the FM- or MFM-modulated signal turns from "High" to "Low" level, reverse current flows through the head to generate magnetic flux changes in it to write data on the disk. This input signal line is valid only when the WRITE GATE and DRIVE SELECT input signal lines are low and the WRITE PROTECT output signal line is high.
5.6 Write Circuit and Erase Circuit

![Block diagram of write circuit and erase circuit]

(1) Write Circuit

The block diagram for the write circuit and erase circuit is shown above.

The write data modulated in the FM or MFM system is divided by the data latch (flip flop) to become a WRITE DATA pulse. The write amplifier output signal becomes a rectangular signal that is inverted by this WRITE DATA pulse. In other words, the write amplifier inverts the polarity of the head current through this signal to cause the magnetic flux synchronized with the WRITE DATA pulse to be generated in the gap of the read/write head and the media is saturation-magnetized and recorded.

The write power gate opens only when the WRITE PROTECT output signal line is high and the WRITE GATE and DRIVE SELECT input signal lines are low, enabling writing and erasing.
The timing chart for the write circuit is shown below.

WRITE GATE

WRITE DATA

Flip Flop (+)

Flip Flop (-)

Write Amplifier
(Write Current)
(2) Erase Circuit

The timing chart for the erase circuit is shown below.

```
WRITE GATE

| tl |

Erase Amplifier

| Output |

| t2 |

Common Driver
```

The tunnel erase system is adopted for this FDD. It consists of a broad-width read/write head followed by a tunnel erase head designed to allow the inner dimension to have the recording information track width. The information once recorded through the read/write head is trimmed at both edges by the tunnel erase head to be shaped to the desired track width. By doing this, even if track divergence occurs, it will not interfere with the adjacent track because the signals for the information track width are efficiently secured by the broad-width read/write head, thus securing the S/N ratio and improving the track density.
For this reason, the erase amplifier output signal rises $t_1$ seconds (minimum time required for the location written on the disk by the read/write head to reach the erase head) after the WRITE gate signal turns from "High" to "Low" level, causing current to flow through the erase head to perform DC erasing. Then, the erase amplifier output signal falls $t_2$ seconds (maximum value of time difference of above $t_1$) after the completion of writing on the media (when the WRITE GATE signal rises), thereby completing the DC erasing.

$t_1$ and $t_2$ seconds are software-determined by the delay circuit.
5.7 MOTOR ON Signal

A spindle motor drive signal appears on this input signal line. When the input signal is low, the spindle motor turns. The disk should be inserted or taken out while the spindle motor is turning. Conversely, when the signal is high, the motor stops. This signal line responds regardless of the DRIVE SELECT signal. The start-up time for the spindle motor requires 0.5 seconds.
5.8 Head Load Circuit (Option)

This circuit assumes the head load state only when the HEAD LOAD signal is low, LSI (IC8) is ready (the media is turning), and signal 05 is low, enabling reading or writing of data. The use of this input signal line requires a setup time for the magnet. This function is available in the two-side type only. When no media is set, head loading is not performed.
6. OUTPUT SIGNAL LINE

6.1 Index/Sector Circuit

The index/sector circuit is configured as shown above.

When the index sensor detects the index hole in the disk, this output signal line goes low indicating the beginning of a track.

The waveform of TP1, pin 2, while the media is turning is shown below.
6.2 Track 00 Detection Circuit

The track 00 detection circuit is configured as shown above.

This circuit detects track 00 which is the outermost track of the disk, and the detected signal is loaded into IC8. The "Low" level signal at the time of track 00 is inputted to R1 of IC8, the "High" level signal in other cases.

When the carrier is at a track other than track 00, the light of the interrupter LED strikes the phototransistor, causing the output signal line to be at a "High" level.
When the carrier is positioned over track 00, the light of the LED is cut off, the "Low" signal is inputted to IC8.
The waveform at TP1, pin 5, is shown below.

* The t varies according to the specification.
This circuit is provided to prevent erroneous erasing of protected data recorded on the disk. The "Low" level signal is outputted when the write enable notch of the disk, inserted into the FDD, is covered with a label, thus disabling writing to the disk. Conversely, when the "High" level signal is outputted, the write enable state is assumed.
This READY signal line is optional in the FB-503-504. When the inserted disk is turning, the output signal line goes low. Consequently, two items, the disk inserted and turning conditions, can be checked by this signal line.

The following waveform appears at check pin TP1, pin 1. The "High" level of this waveform indicates the Busy state, and the "Low" level the Ready state. When the index detection circuit detects the index, the signal turns from a "High" to a "Low" level.
6.5 Read Amplifier Circuit

The block diagram for the read amplifier is shown above.

This circuit picks up data recorded on the media through the magnetic head, and outputs read data close to the recorded signals by amplifying, although it slightly deviates time-wise, identifying, and pulse-shaping the data.

The timing chart for the read amplifier circuit is shown below.

Low Pass Filter Output(+) *TP3

Low Pass Filter Output(-) *TP4

Differentiator Output(+) Saddle

Differentiator Output(-) Zero close Point

Comparator Output

Pulse Shaping Output (READ DATA) *TP1 - TP2 (GND)
CHAPTER 4  

Circuit Diagram

(FB-500 Series)
Chapter 5 Troubleshooting

(FB-500 Series)
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<th>Topic</th>
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<tbody>
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<tr>
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<td>5-11</td>
</tr>
<tr>
<td>READ CIRCUIT</td>
<td>5-13</td>
</tr>
</tbody>
</table>
1. Soft Error Processing

1.1 General

The following soft errors are often mistakenly for errors caused by troubles or mis-adjustments of the disk drive.

- Errors caused by improper operational procedure, incorrect programming or damaged disk.
- Software error caused by dust in the air, random electric interference or other external cause.

Unless a defective assembly point or damage point is clearly found in visual inspection, check to see whether the error repeats with the current diskette and also whether the same error is caused with other diskette.

1.2 Detection and Correction and Read Error

Read errors are usually caused by the following conditions.

1. Dust between the read/write head and disk; usually dirt resulting from dust is eliminated by the self-cleaning wiper in the diskette.
2. Fine track divergence which is not detected during writing.
3. Wear of damaged load pad or wear of disk caused by side 0 or side 1 of double-side head.
4. Improper grounding of the power supply of the disk drive in the host computer.
5. Improper motor speed.

To correct soft errors as above (1) to (5), follow the steps below.

1. Re-read the error-occurred track about 10 times.
2. If the data is not restored in step 1, allow the head to move to track 00 and make sure that the head is at track 00.
3. Move the head to the error-occurred track.
4. Repeat step (1).
5. Errors which cannot be corrected by repeating the above steps are unrecoverable errors.
1.3 Write Error

An error which has occurred during writing is detected during a subsequent reading of the data written.

(1) To eliminate the error, write and read again.

(2) If the error still occurs after the above procedure is repeated a few times, perform reading using another track to determine whether the disk or drive is malfunctioning.

(3) If the error persists, change the disk and perform the above procedure.
   If the error still persists, the drive is defective.

1.4 Seek Error

Possible Cause.

(1) The pulse motor or pulse motor drive circuit is defective.

(2) The carriage is defective.

There are two procedures to correct seek errors.

(1) Readjust the belt tension. Refer to Chapter 2.

(2) Readjust track 00. Refer to Chapter 2.

1.5 Interchange Error

Sometimes data written by a disk drive cannot be read by another drive. This phenomenon is called "interchange error". The points to be checked are:

(1) Head alignment is defective. Refer to Head/Radial Adjustment.

(2) Head output is not enough. Refer to Head Output Adjustment.

(3) The motor speed is incorrect. Refer to Motor Speed Adjustment.

(4) Check the center hole of the disk.
   If the center hole of the disk is damaged, check the clamp mechanism.
2. FLOPPY DISK DRIVE FOR REPAIR

2.1 Have the user send you the defective floppy disk drive together with the diskette which was used when the user found it defective. Without this diskette, you may fail to locate the trouble.

2.2 Be sure to get information from the user about the operating conditions at the time the user found the floppy disk drive defective. This will help in troubleshooting later.

   a) If the Active lamp will not light and the unit does not operate at all, check the DC Power Supply.

   b) If the Active lamp lights but an operating sound is not heard inside the unit, proceed to section 2.1.

   c) If stepper motor turns without causing carriage movement, proceed to section 2.

   d) If the drive executes continuously but fails to read and write, proceed to sections 2.2 and 2.3.
Sample Test Connection

Drive 0: Normal Drive

Drive 1: Sample Drive
3. TROUBLESHOOTING PROCEDURES

START

Connect the sample as shown in the figure on the preceding page.

Turn on the units in the order of drive 0, drive 1 (sample), CRT and host computer.

Insert the diskette with a diskette exerciser program into the drive 0, and lock the door. Insert a work disk into the drive 1, and lock the door.

Select the drive, and turn on the hub motor to restore the head to Track 00.

Does the Active lamp light?  
Yes  

Is the index pulse present? (TP1-pin 2)  
Yes  

Is there a track 0 Signal? (TP1-Pin 5)  
Yes  

Check the power unit.  

No  

Go to the media rotation check routine.  

No  

Go to the tracking mechanism check routine.

No

Initialize track 0 of drive 1 and read it continuously.

CONT'D ON NEXT PAGE
The sample of drive 1 is normal. The diskette of the user is defective.

Check the compatibility.
START

Is the motor on signal LOW?

Yes

Will the motor turn at all?

No

Is the DC supply normal?

Yes

Replace IC6

Is the set screw of the DD motor loose?

Yes

Retighten the set screw

No

Replace or repair the connector

Is there a media slip?

No

Yes

Replace the clamp

Is the voltage of Bl on CN5-pin 3 at 12V?

Yes

Replace the DD motor.

No

Adjust the media rotation speed

Replace IC4

Is TP1-pin 12 outputting a pulse signal?

No

Is a pulse signal output from pin 8 on the interface connector?

Yes

Replace the drive PCB

No

Is pin 11 on IC7 at high level?

Yes

Replace IC7

No

Is the voltage of IC6-pin 10 at 0.4V?

Yes

Is the collect or output of Q3 at high level?

No

Replace Q3

Yes

Replace IC6

Is pin 2 on CN-7 at high level?

Yes

Replace the index sensor or DD motor

No

Adjust the index burst time

Replace IC4

The interface or cable of the host computer is defective
3.1 Tracking Mechanism (Track 0 Signal Won't Be Generated)

START

Is tracking performed at all?
Yes -> A
No

Can a stepping signal be input?
No
Yes

Is the DC supply normal?
No
Yes

Are the output of pins 3, 4, 5, 6 on CN-3 normal?
No
Yes

Turn off the power switch and move the carrier by hand in both directions

Is the carrier movement smooth?
No
Replace the carrier.
Yes

Is the steel belt broken or the set screw loose?
No
Adjust or replace the steel belt.
Yes

Replace the pulse motor.

Adjust CE by using the alignment diskette.

The interface cable of the host computer is defective
Check the DC supply

Replace the carrier.

Excessive tensioning of the head cable.
A

Is the collector of Q2 at low level when black paper is inserted into the track 00 detector?

Yes

Is pin 2 on CN-8 at high level before the carrier touches the 0 stopper?

Yes

Adjust the position of the interrupter

No

Is pin 2 on CN-8 at low level?

Yes

Is pin 2 on CN-8 at high level before the carrier touches the 0 stopper?

No

Replace IC11

Is an output generated on the interface connector?

Yes

The interface or cable of the host computer is defective

No

Replace IC2 or IC5

Replace the interrupter
Are the waveforms of pins 1-4 of IC6 normal? No

Are a high or low step pulse outputted at pin 9 of IC1? No

Is C1 defective.

Yes

C6 is defective.
3.2 Write Circuit Check

START

Is write data input to pin 22 on CN-4?  
No  
Yes  

Is pin 24, write gate on CN-4 at low level?  
No  
Yes  

Is pin 6 on IC5 at high level?  
No  
Yes

Is pin 28 on CN-4 at low level?  
Yes  
No

Is any of the DS signal (pin 6, 10, 12 or 14) at low level?  
Yes  
No

Is short pin on SW1 correctly selected?  
No  
Yes

Do the levels of H and L appear at 8th pin of IC9 alternately with those at 9th pin?  
No  
Yes

Does the level at pin 11 of IC9 change as H or L?  
Yes  
No

Replace IC9

The interface of the host computer or the cable is defective.

Replace IC4

Write protect state
Check the Notch of media.

Connect the shot pin to the DS signal terminal
Is pin 3 on RA5 at 12V? No

Is pin 2 on RA6 at 12V? No

Replace L1 or check the DC power supply unit

Is pin 1 on RA6 at 0.7V? No

Replace D4, Q4 or Q8.

Do the level of Q5 become H and L (on and 1ff) alternately with the level of Q6? No

Will pin 1 and 4 on RA5 turn High and Low? Check with oscilloscope.

Replace IC10

Replace the carrier assembly

Adjust the head alignment
Read Circuit Malfunction

START

Does an output waveform appear at pins 16 and 17 of IC12?
Yes

No

IC12 or head is defective.

Does a differential waveform appear at pins 3 and 4 of TP2?
Yes

No

Q9 or Q10 is defective.

Yes

IC12 is defective.

Does a read waveform appear at pin 1 of TP2?
Yes

No

IC2 or IC5 is defective

Does a read waveform appear at pin 3 of IC2?
Yes

The interface of the most computer of the cable is defective.
CHAPTER 6        Parts List

(FB-500 Series)

DOCUMENT NO. E5-2125
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CHAPTER 7  RECOMMENDED SPARE PARTS LIST

(FB-500 Series)
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