M5M4256P-12, -15, -20

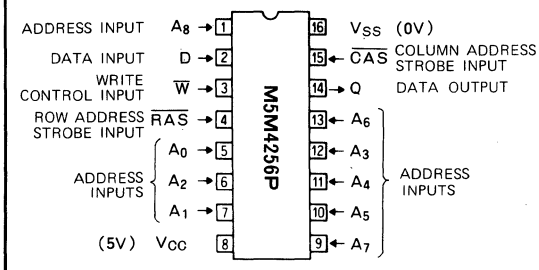
262 144-BIT (262 144-WORD BY 1-BIT) DYNAMIC RAM

NEW PRODUCT

DESCRIPTION

This is a family of 262 144-word by 1-bit dynamic RAMs, fabricated with the high performance N-channel silicon gate MOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities. In addition to the $\overline{RAS}$ only refresh mode, the Hidden refresh mode and $\overline{CAS}$ before $\overline{RAS}$ refresh mode are available.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FEATURES

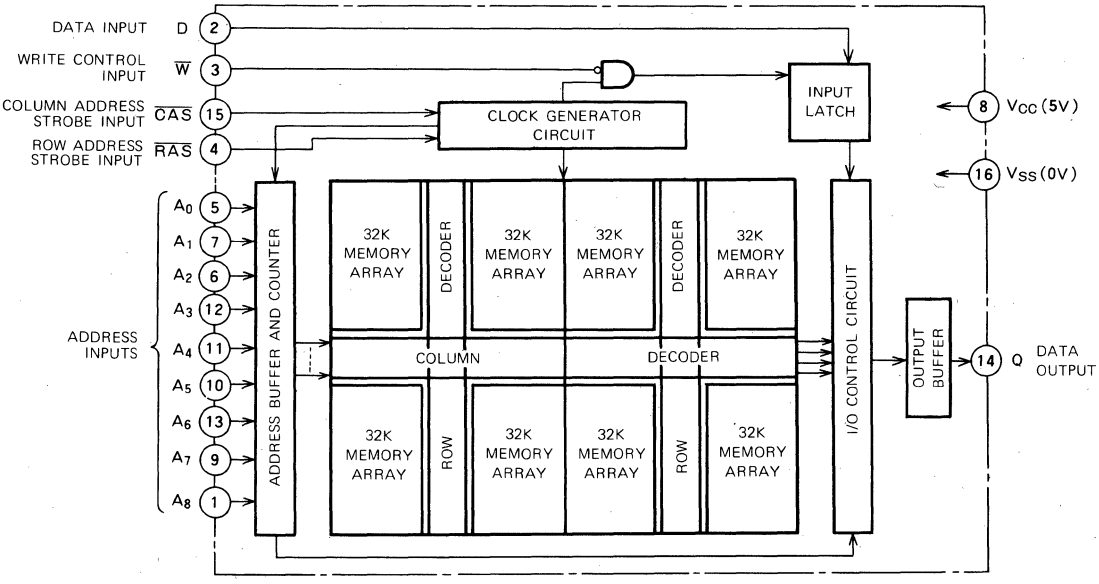
Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5M4256P-12	120	230	260
M5M4256P-15	150	260	230
M5M4256P-20	200	330	190

- Standard 16-pin package
- Single 5V±10% supply
- Low standby power dissipation: 25mW (max)
- Low operating power dissipation:
  - M5M4256P-12 . . . . . 360mW (max)
  - M5M4256P-15 . . . . . 330mW (max)
  - M5M4256P-20 . . . . . 275mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability
- Read-modify-write, $\overline{RAS}$-only-refresh, Page-mode capabilities
- $\overline{CAS}$ before $\overline{RAS}$ refresh mode capability
- All input terminals have low input capacitance and are directly TTL-compatible
- Output is three-state and directly TTL-compatible
- 256 refresh cycles every 4ms. Pin 1 is not needed for refresh.
- $\overline{CAS}$ controlled output allows hidden refresh

APPLICATION

- Main memory unit for computers
- Microcomputer memory

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION

The M5M4256P provides, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	D	Row address	Column address	Q		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	*
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	DNC	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open.
* : Page mode identical except refresh is No.

SUMMARY OF OPERATIONS

Addressing

To select one of the 262 144 memory cells in the M5M4256P the 18-bit address signal must be multiplexed into 9 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 9 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 9 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d\,(RAS\text{-}CAS)}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(RAS\text{-}CAS)\,max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations, e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(RAS\text{-}CAS)}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$, which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of $\overline{W}$ input and $\overline{CAS}$ input. Thus when the $\overline{W}$ input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the $\overline{W}$ input makes its negative transition after $\overline{CAS}$, the $\overline{W}$ negative transition is set as the reference point for setup and hold times.

Data Output Control

The output of the M5M4256P is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$.

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5M4256P, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2 Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 512 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

Each of the 256 rows ($A_0 \sim A_7$) of the M5M4256P must be refreshed every 4 ms to maintain data. The methods of refreshing for the M5M4256P are as follows.

1. Normal Refresh

Read cycle and Write cycle (early write, delayed write or read-modify-write) refresh the selected row as defined by the low order ($\overline{RAS}$) addresses. Any write cycle, of course, may change the state of the selected cell. Using a read, write, or read-modify-write cycle for refresh is not recommended for systems which utilize "wired-OR" outputs since output bus contention will occur.

2. $\overline{RAS}$ Only Refresh

In this refresh method, the $\overline{CAS}$ clock should be at a V_{IH} level and the system must perform $\overline{RAS}$ Only cycle on all 256 row address every 4 ms. The sequential row addresses from an external counter are latched with the $\overline{RAS}$ clock and associated internal row locations are refreshed. A $\overline{RAS}$ Only Refresh cycle maintains the output in the high impedance state with a typical power reduction of 20% over a read or write cycle.

3. $\overline{CAS}$ before $\overline{RAS}$ Refresh

If $\overline{CAS}$ falls $t_{SUR(CAS-RAS)}$ earlier than $\overline{RAS}$ and if $\overline{CAS}$ is kept low by $t_{hR(RAS-CAS)}$ after $\overline{RAS}$ falls, $\overline{CAS}$ before $\overline{RAS}$ Refresh is initiated. The external address is ignored and the refresh address generated by the internal 8-bit counter is put into the address buffer to refresh the corresponding row. The output will stay in the high impedance state.

If $\overline{CAS}$ is kept low after the above operation, $\overline{RAS}$ cycle initiates $\overline{RAS}$ Only Refresh with internally generated refresh address (Automatic refresh). The output will again stay in the high impedance state.

Bringing $\overline{RAS}$ high and then low while $\overline{CAS}$ remains high initiates the normal $\overline{RAS}$ Only Refresh using the external address.

If $\overline{CAS}$ is kept low after the normal read/write cycle, $\overline{RAS}$ cycle initiates the $\overline{RAS}$ Only Refresh using the internal refresh address and especially after the normal read cycle, it becomes Hidden Refresh with internal address. The output is available unit $\overline{CAS}$ is brought high.

4. Hidden Refresh

A feature of the M5M4256P is that refresh cycles may be performed while maintaining valid data at the output pin by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as hidden refresh.

Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period, executing a $\overline{RAS}$-only cycling, but with $\overline{CAS}$ held low.

The advantage of this refresh mode is that data can be held valid at the output data port indefinitely by leaving the $\overline{CAS}$ asserted. In many applications this eliminates the need for off-chip latches.

Power Dissipation

Most of the circuitry in the M5M4256P is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5M4256P as chip-select in the memory system, but if $\overline{RAS}$ is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

The M5M4256P operates on a single 5V power supply.

A wait of some 500μs and eight or more dummy cycles is necessary after power is applied to the device before memory operation is achieved.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1～7	V
V_I	Input voltage		−1～7	V
V_O	Output voltage		−1～7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta＝25°C	1000	mW
Topr	Operating free-air temperature range		0～70	°C
Tstg	Storage temperature range		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage, all inputs	−2		0.8	V

Note 1: All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±10%, V_{SS}＝0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}＝−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}＝4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦V_{CC}, Other input pins ＝0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M4256P-12	$\overline{RAS}$, $\overline{CAS}$ cycling t_{CR}＝t_{CW}＝ min, output open			65	mA
		M5M4256P-15				60	mA
		M5M4256P-20				50	mA
I_{CC2}	Supply current from V_{CC}, standby		$\overline{RAS}$＝$\overline{CAS}$＝V_{IH} output open			4.5	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M4256P-12	$\overline{RAS}$ cycling $\overline{CAS}$＝V_{IH} $t_{C(\overline{RAS})}$＝ min, output open			55	mA
		M5M4256P-15				50	mA
		M5M4256P-20				40	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 3, 4)	M5M4256P-12	$\overline{RAS}$＝V_{IL}, $\overline{CAS}$ cycling t_{CPG}＝ min, output open			50	mA
		M5M4256P-15				45	mA
		M5M4256P-20				40	mA
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M4256P-12	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{C(\overline{RAS})}$ = min, output open			60	mA
		M5M4256P-15				55	mA
		M5M4256P-20				45	mA
$C_{I(A)}$	Input capacitance, address inputs		V_I＝V_{SS} f＝1MHz V_i＝25mVrms			5	pF
$C_{I(D)}$	Input capacitance, data input					5	pF
$C_{I(W)}$	Input capacitance, write control input					7	pF
$C_{I(RAS)}$	Input capacitance, $\overline{RAS}$ input					10	pF
$C_{I(CAS)}$	Input capacitance, $\overline{CAS}$ input					10	pF
C_O	Output capacitance		V_O＝V_{SS}, f＝1MHz, V_i＝25mVrms			7	pF

Note 2: Current flowing into an IC is positive; out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted, See notes 5, 6 and 7)

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4256P-12		M5M4256P-15		M5M4256P-20		
				Min	Max	Min	Max	Min	Max	
t_{CRF}	Refresh cycle time		t_{REF}		4		4		4	ms
$t_{W(RASH)}$	$\overline{RAS}$ high pulse width		t_{RP}	100		100		120		ns
$t_{W(RASL)}$	$\overline{RAS}$ low pulse width		t_{RAS}	120	10000	150	10000	200	10000	ns
$t_{W(CASL)}$	$\overline{CAS}$ low pulse width		t_{CAS}	60		75		100		ns
$t_{W(CASH)}$	$\overline{CAS}$ high pulse width	(Note 8)	t_{CPN}	30		35		40		ns
$t_{h(RAS-CAS)}$	$\overline{CAS}$ hold time after $\overline{RAS}$		t_{CSH}	120		150		200		ns
$t_{h(CAS-RAS)}$	$\overline{RAS}$ hold time after $\overline{CAS}$		t_{RSH}	60		75		100		ns
$t_{d(CAS-RAS)}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$	(Note 9)	t_{CRP}	30		30		40		ns
$t_{d(RAS-CAS)}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$	(Note 10)	t_{RCD}	20	60	25	75	30	100	ns
$t_{su(RA-RAS)}$	Row address setup time before $\overline{RAS}$		t_{ASR}	0		0		0		ns
$t_{su(CA-CAS)}$	Column address setup time before $\overline{CAS}$		t_{ASC}	−5		−5		−5		ns
$t_{h(RAS-RA)}$	Row address hold time after $\overline{RAS}$		t_{RAH}	15		20		25		ns
$t_{h(CAS-CA)}$	Column address hold time after $\overline{CAS}$		t_{CAH}	20		25		35		ns
$t_{h(RAS-CA)}$	Column address hold time after $\overline{RAS}$		t_{AR}	80		100		135		ns
t_{THL} t_{TLH}	Transition time		t_T	3	50	3	50	3	50	ns

Note 5: An initial pause of 500μs is required after power-up followed by any eight $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved.
6: The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.
7: Reference levels of input signals are $V_{IH\ min.}$ and $V_{IL\ max.}$ Reference levels for transition time are also between V_{IH} and V_{IL}.
8: Except for page-mode.
9: $t_{d(CAS-RAS)}$ requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.
10: Operation within the $t_{d(RAS-CAS)}$ max limit insures that $t_{a(RAS)}$ max can be met. $t_{d(RAS-CAS)max}$ is specified reference point only; if $t_{d(RAS-CAS)}$ is greater than the specified $t_{d(RAS-CAS)}$ max limit, then access time is controlled exclusively by $t_{a(CAS)}$.
$t_{d(RAS-CAS)min} = t_{h(RAS-RA)min} + 2t_{THL(tTLH)} + t_{su(CA-CAS)min}$.

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Read Cycle

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4256P-12		M5M4256P-15		M5M4256P-20		
				Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time		t_{RC}	230		260		330		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		0		0		ns
$t_{h(CAS-R)}$	Read hold time after $\overline{CAS}$	(Note 11)	t_{RCH}	0		0		0		ns
$t_{h(RAS-R)}$	Read hold time after $\overline{RAS}$	(Note 11)	t_{RRH}	20		20		25		ns
$t_{dis(CAS)}$	Output disable time	(Note 12)	t_{OFF}	0	35	0	40	0	50	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 13)	t_{CAC}		60		75		100	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 14)	t_{RAC}		120		150		200	ns

Note 11: Either $t_{h(RAS-R)}$ or $t_{h(CAS-R)}$ must be satisfied for a read cycle.
12: $t_{dis(CAS)max}$ defines the time at which the output achieves the open circuit condition and is not reference to V_{OH} or V_{OL}.
13: This is the value when $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$. Test conditions; Load = 2TTL, C_L = 100pF
14: This is the value when $t_{d(RAS-CAS)} < t_{d(RAS-CAS)max}$. When $t_{d(RAS-CAS)} \geqq t_{d(RAS-CAS)max}$, $t_{a(RAS)}$ will increase by the amount that $t_{d(RAS-CAS)}$ exceeds the value shown. Test conditions; Load = 2TTL, C_L = 100pF

Write Cycle

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4256P-12		M5M4256P-15		M5M4256P-20		
				Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time		t_{RC}	230		260		330		ns
$t_{su(W-CAS)}$	Write setup time before $\overline{CAS}$	(Note 17)	t_{WCS}	−10		−10		−10		ns
$t_{h(CAS-W)}$	Write hold time after $\overline{CAS}$		t_{WCH}	40		45		55		ns
$t_{h(RAS-W)}$	Write hold time after $\overline{RAS}$		t_{WCR}	100		120		155		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	40		45		55		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	40		45		55		ns
$t_{w(W)}$	Write pulse width		t_{WP}	40		45		55		ns
$t_{su(D-CAS)}$	Data-in setup time before $\overline{CAS}$		t_{DS}	0		0		0		ns
$t_{h(CAS-D)}$	Data-in hold time after $\overline{CAS}$		t_{DH}	30		35		40		ns
$t_{h(RAS-D)}$	Data-in hold time after $\overline{RAS}$		t_{DHR}	90		110		140		ns

Read, Write and Read-Modify-Write Cycles

Symbol	Parameter		Alternative Symbol	Limits						Unit
				M5M4256P-12		M5M4256P-15		M5M4256P-20		
				Min	Max	Min	Max	Min	Max	
t_{CRW}	Read-write cycle time	(Note 15)	t_{RWC}	260		295		370		ns
t_{CRMW}	Read-modify-write cycle time	(Note 16)	t_{RMWC}	275		310		390		ns
$t_{h(W-RAS)}$	$\overline{RAS}$ hold time after write		t_{RWL}	40		45		55		ns
$t_{h(W-CAS)}$	$\overline{CAS}$ hold time after write		t_{CWL}	40		45		55		ns
$t_{w(W)}$	Write pulse width		t_{WP}	40		45		55		ns
$t_{su(R-CAS)}$	Read setup time before $\overline{CAS}$		t_{RCS}	0		0		0		ns
$t_{d(RAS-W)}$	Delay time, $\overline{RAS}$ to write	(Note 17)	t_{RWD}	110		135		180		ns
$t_{d(CAS-W)}$	Delay time, $\overline{CAS}$ to write	(Note 17)	t_{CWD}	50		60		80		ns
$t_{su(D-W)}$	Data-in set-up time before write		t_{DS}	0		0		0		ns
$t_{h(W-D)}$	Data-in hold time after write		t_{DH}	40		45		55		ns
$t_{dis(CAS)}$	Output disable time		t_{OFF}	0	35	0	40	0	50	ns
$t_{a(CAS)}$	$\overline{CAS}$ access time	(Note 13)	t_{CAC}		60		75		100	ns
$t_{a(RAS)}$	$\overline{RAS}$ access time	(Note 14)	t_{RAC}		120		150		200	ns

Note 15. t_{CRW} min is defined as $t_{CRW}\,min = t_{d(RAS-CAS)}\,max + t_{d(CAS-W)}\,min + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

16. t_{CRMW} min is defined as $t_{CRMW}\,min = t_{a(RAS)}\,max + t_{h(W-RAS)} + t_{w(RASH)} + 3t_{TLH(tTHL)}$

17. $t_{su(W-CAS)}$, $t_{d(RAS-W)}$, and $t_{d(CAS-W)}$ do not define the limits of operation, but are included as electrical characteristics only.

When $t_{su(W-CAS)} \geqq t_{su(W-CAS)}\,min$, an early-write cycle is performed, and the data output keeps the high-impedance state.

When $t_{d(RAS-W)} \geqq t_{d(RAS-W)}\,min$, and $t_{d(CAS-W)} \geqq t_{su(W-CAS)}\,min$ a read-write cycle is performed, and the data of the selected address will be read out on the data output.

For all conditions other than those described above, the condition of data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-12		M5M4256P-15		M5M4256P-20		
			Min	Max	Min	Max	Min	Max	
t_{CPG}	Page-mode cycle time	t_{PC}	125		145		190		ns
$t_{w(CASH)}$	$\overline{CAS}$ high pulse width	t_{CP}	55		60		80		ns
t_{CPGRW}	Page-mode RW cycle time	t_{PCRW}	160		180		230		ns
t_{CPGRMW}	Page-mode RMW cycle time	t_{PCRMW}	170		195		250		ns

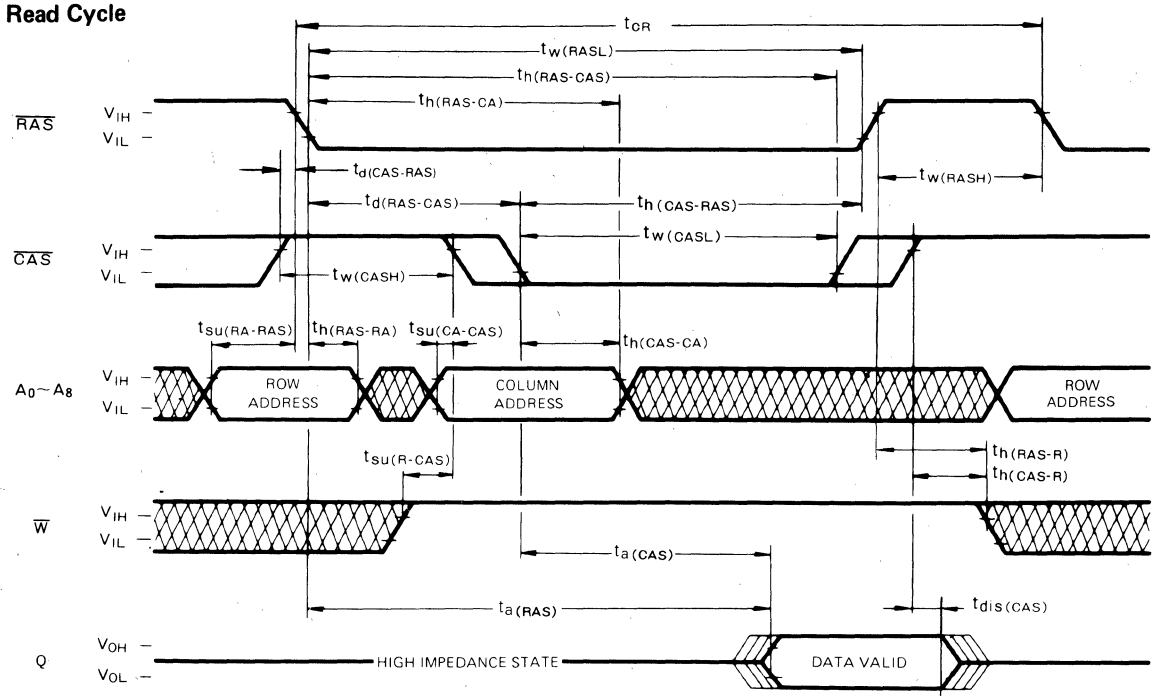
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 18)

Symbol	Parameter	Alternative Symbol	Limits						Unit
			M5M4256P-12		M5M4256P-15		M5M4256P-20		
			Min	Max	Min	Max	Min	Max	
$t_{suR(CAS-RAS)}$	$\overline{CAS}$ setup time for auto refresh	t_{CSR}	30		30		40		ns
$t_{hR(RAS-CAS)}$	$\overline{CAS}$ hold time for auto refresh	t_{CHR}	50		50		50		ns
$t_{dR(RAS-CAS)}$	Precharge to $\overline{CAS}$ active time	t_{RPC}	0		0		0		ns

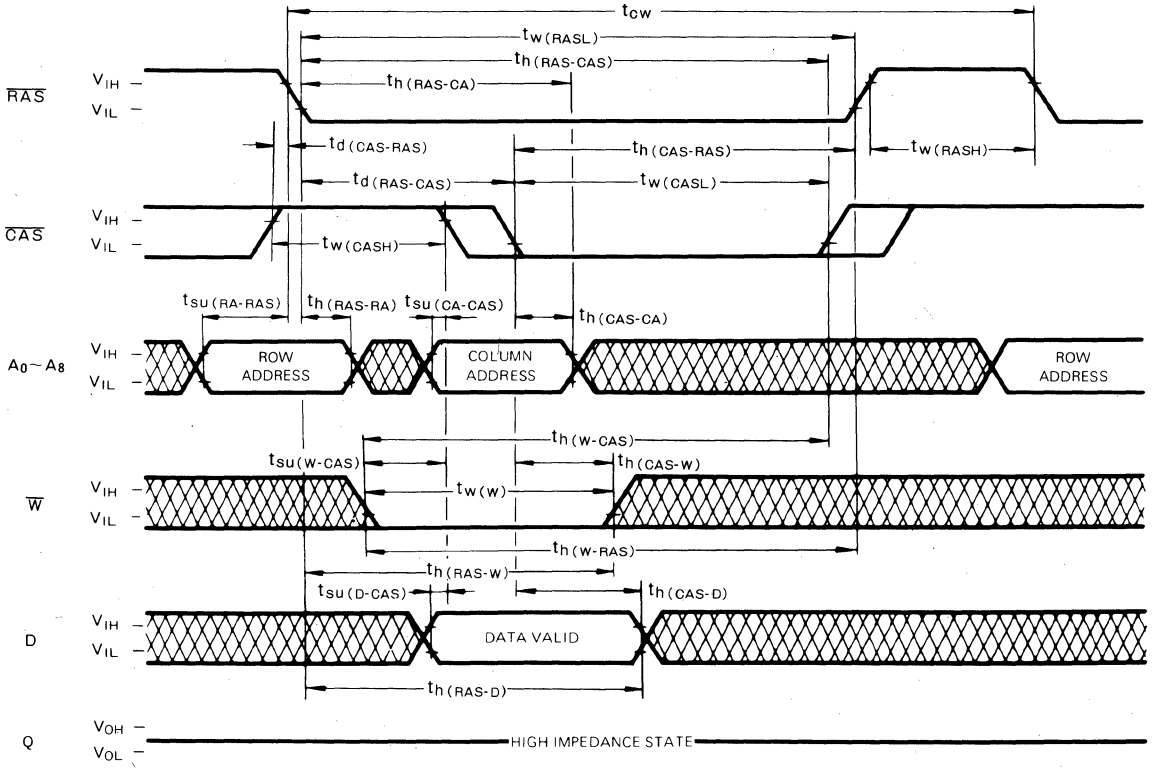
Note 18. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

TIMING DIAGRAMS (Note 19)

Read Cycle

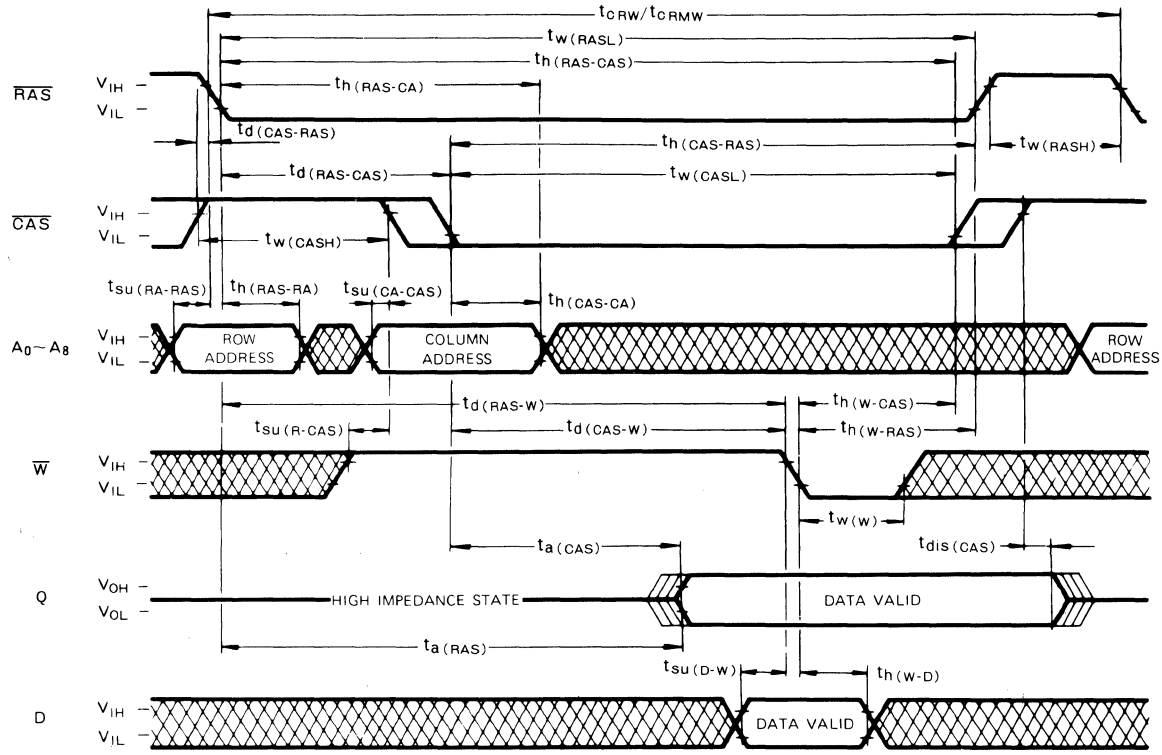


Write Cycle (Early Write) (Note 21)

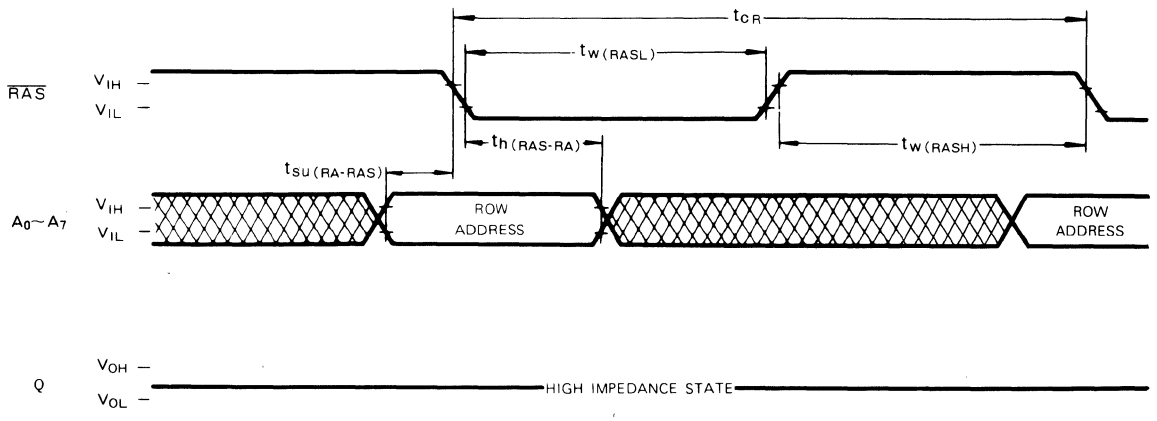


MITSUBISHI ELECTRIC

Read-Write and Read-Modify-Write Cycles



RAS-Only Refresh Cycle (Note 20)

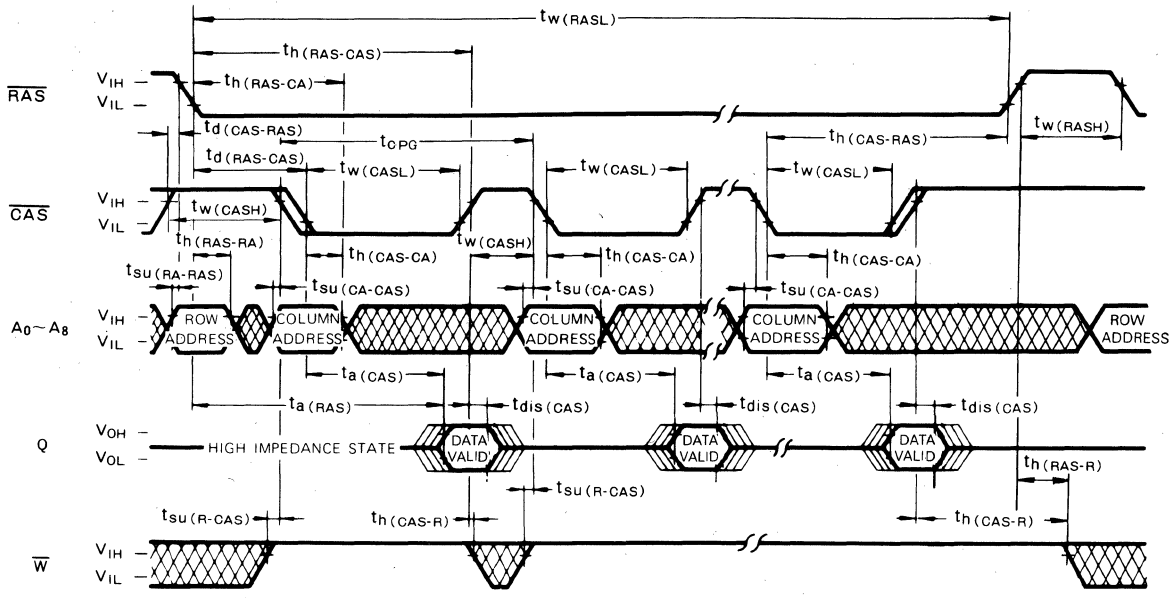


Note 19. Indicates the don't care input

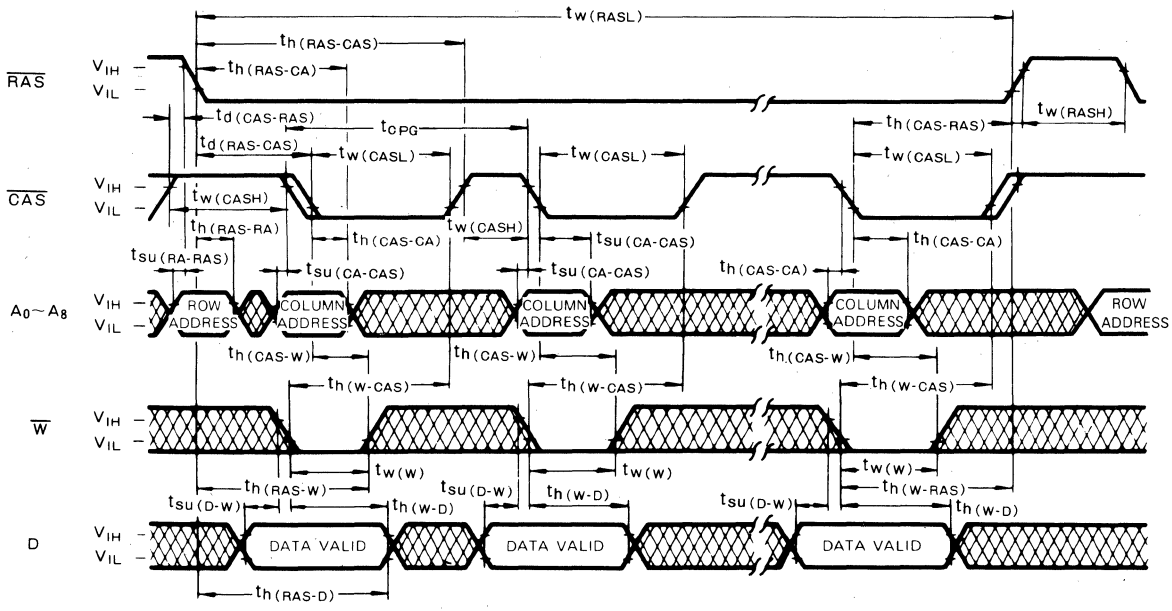
The center-line indicates the high-impedance state

Note 20. $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = don't care.
A_8 may be V_{IH} or V_{IL}.

Page-Mode Read Cycle

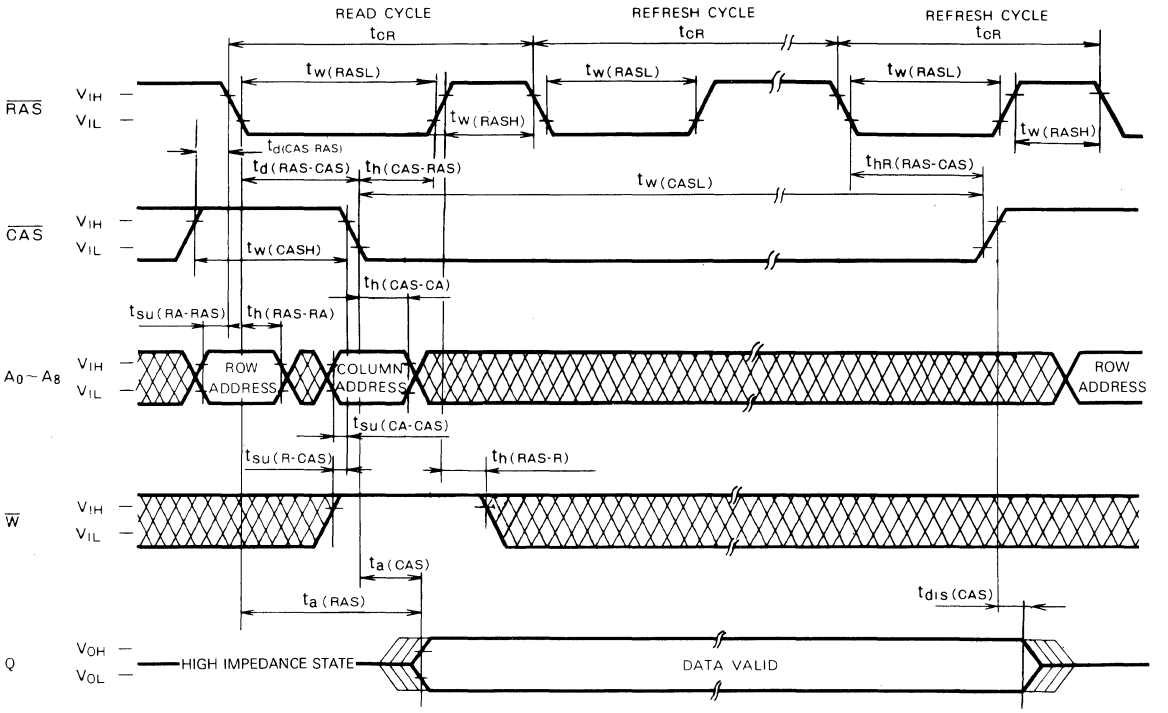


Page-Mode Write Cycle

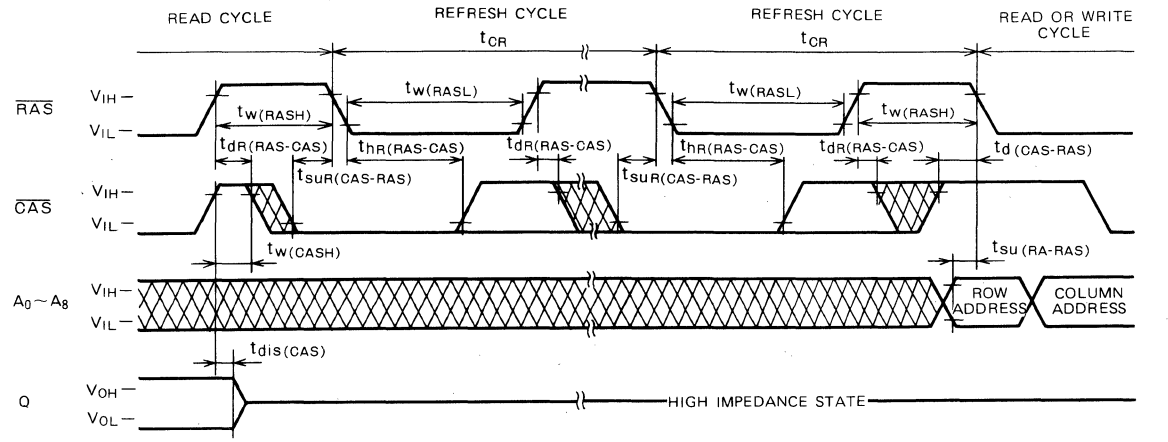


MITSUBISHI ELECTRIC

Hidden Refresh Cycle



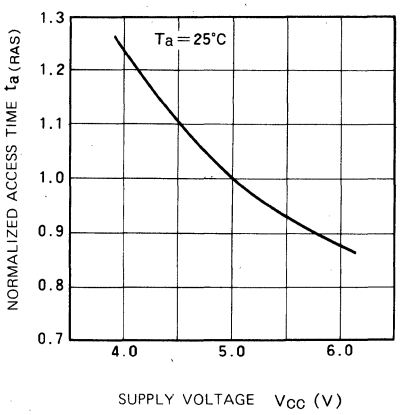
CAS before RAS Refresh Cycle (Note 21)



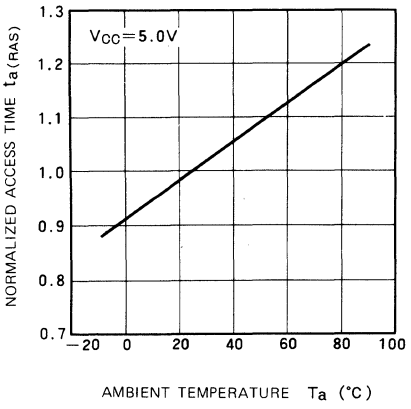
Note 21: W, D = don't care.

TYPICAL CHARACTERISTICS

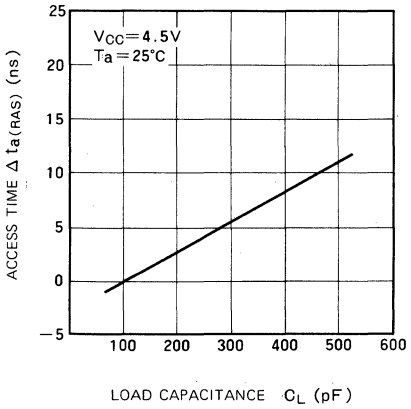
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



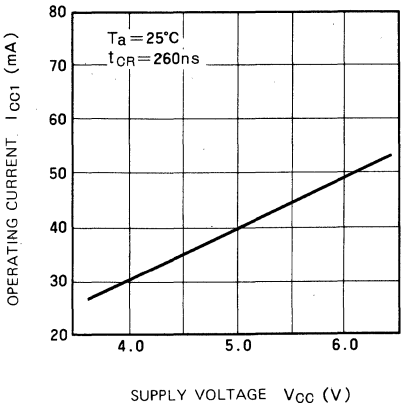
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



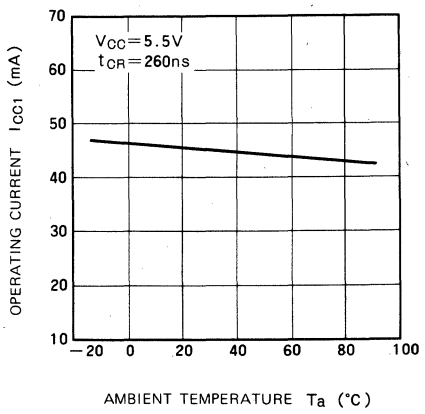
ACCESS TIME VS. LOAD CAPACITANCE



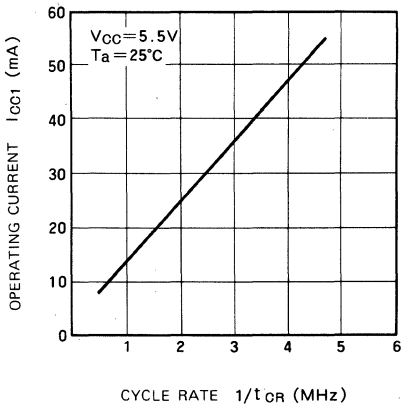
OPERATING CURRENT VS. SUPPLY VOLTAGE



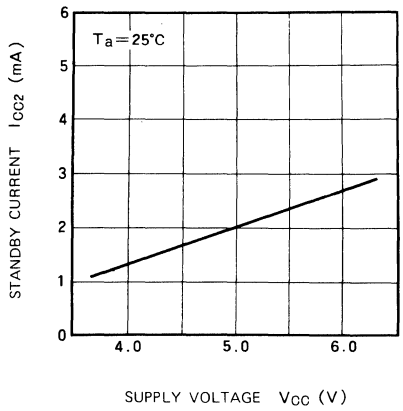
OPERATING CURRENT VS. AMBIENT TEMPERATURE



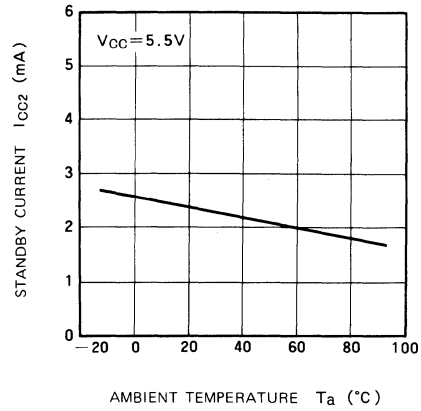
OPERATING CURRENT VS. CYCLE RATE



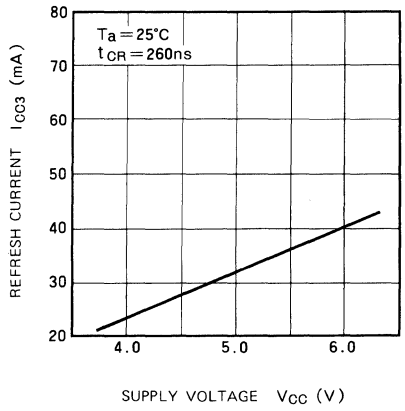
STANDBY CURRENT VS. SUPPLY VOLTAGE



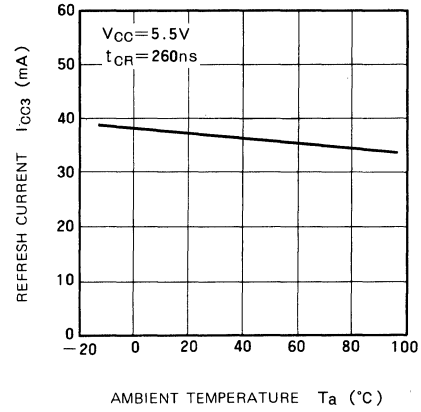
STANDBY CURRENT VS. AMBIENT TEMPERATURE



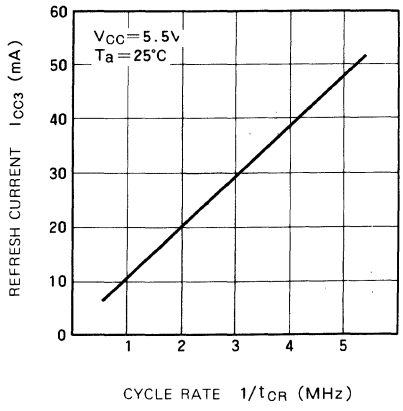
REFRESH CURRENT VS. SUPPLY VOLTAGE



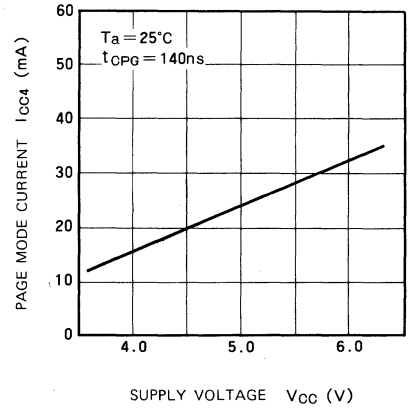
REFRESH CURRENT VS. AMBIENT TEMPERATURE



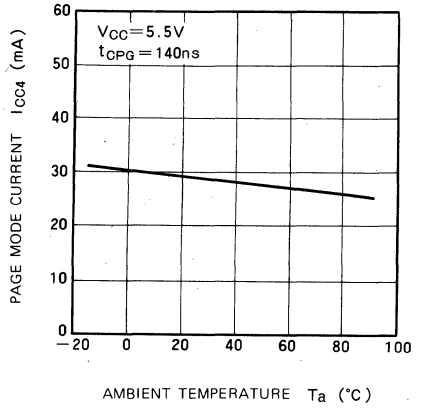
REFRESH CURRENT VS. CYCLE RATE



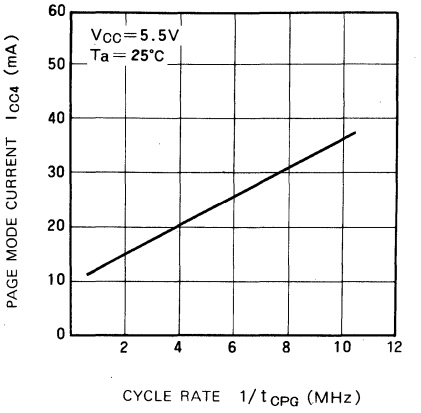
PAGE MODE CURRENT VS. SUPPLY VOLTAGE



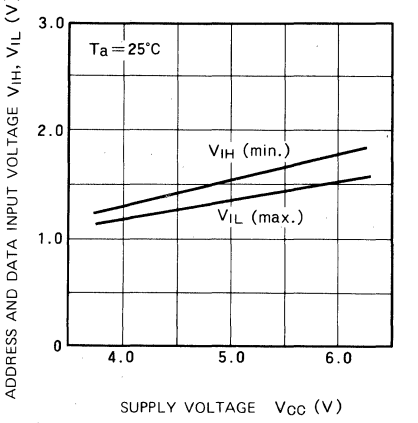
PAGE MODE CURRENT VS. AMBIENT TEMPERATURE



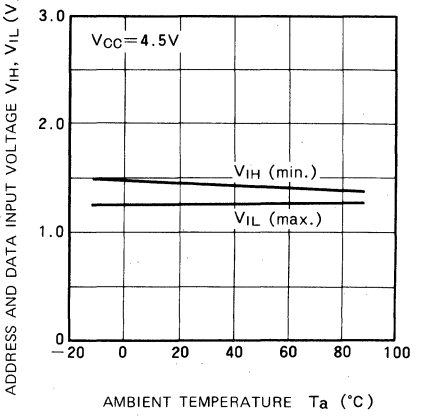
PAGE MODE CURRENT VS. CYCLE RATE



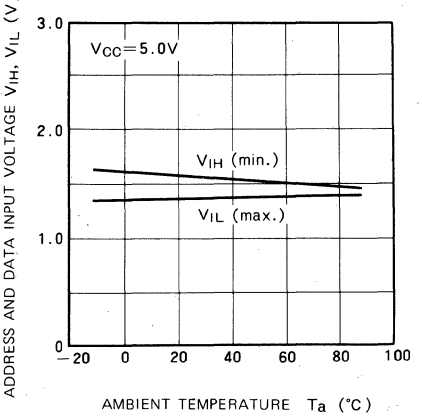
ADDRESS AND DATA INPUT VOLTAGE VS. SUPPLY VOLTAGE



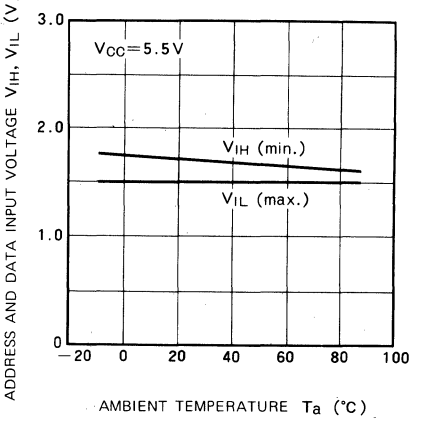
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



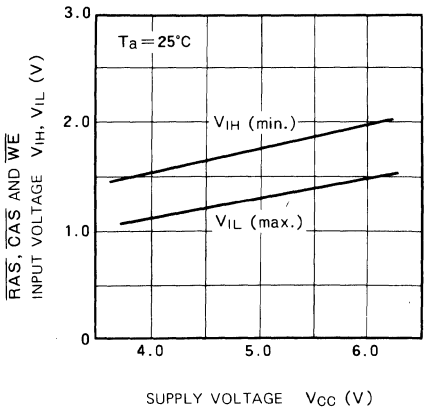
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



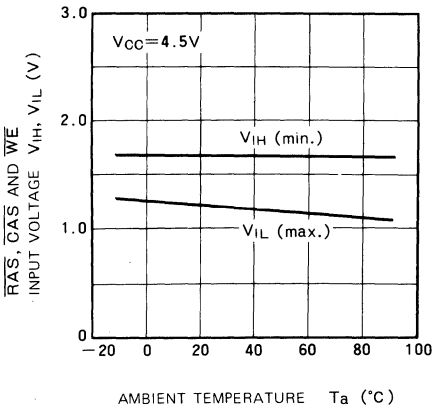
ADDRESS AND DATA INPUT VOLTAGE VS. AMBIENT TEMPERATURE



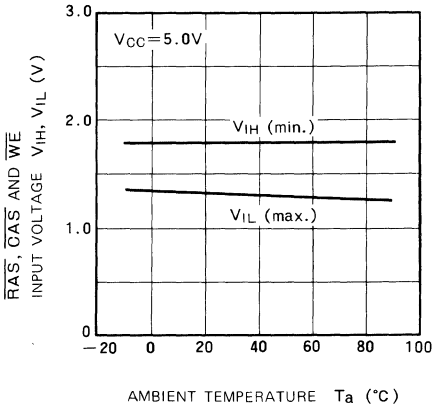
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. SUPPLY VOLTAGE



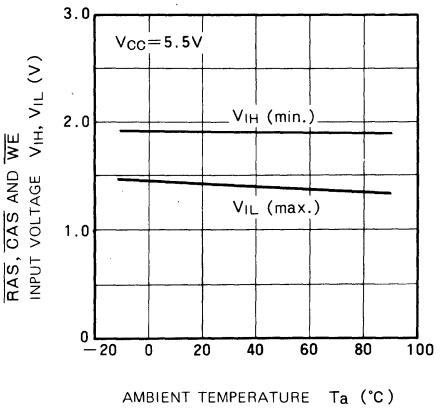
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



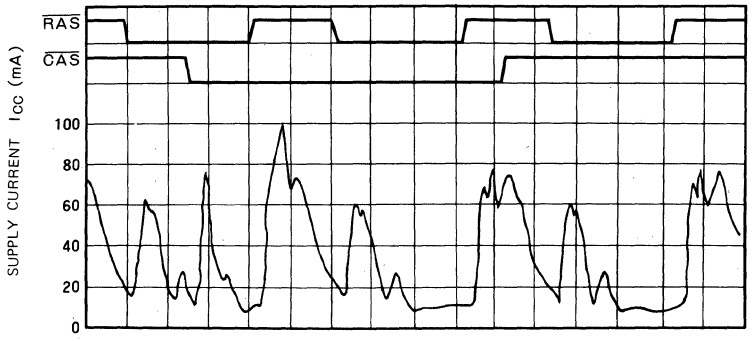
$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE



$\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE VS. AMBIENT TEMPERATURE

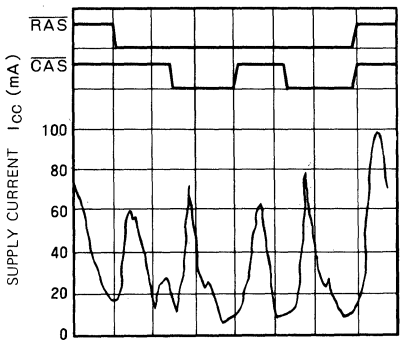


RAS/CAS CYCLE **HIDDEN REFRESH CYCLE** **RAS ONLY REFRESH CYCLE**



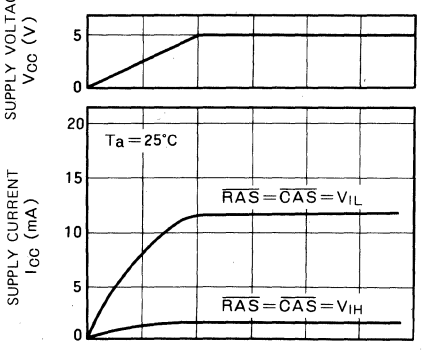
50ns/DIVISION

PAGE MODE CYCLE



50ns/DIVISION

CURRENT WAVEFORM DURING POWER UP



50μs/DIVISION